UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,964	08/28/2003	Razak Hossain	03-LJ-011	1963

34603 7590 05/30/2007
STMICROELECTRONICS, INC
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
05/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/604,964	HOSSAIN, RAZAK	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 20-36* is/are pending in the application.

4a) Of the above claim(s) *20-32 and 34-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/604,964, and Amendment filed on 03/11/2007. Claims 20-36 have been newly added, claim 33 discloses a method, which is identical to claim 1. Claims 4-19 have been cancelled. Claims 1- 3 and 20-36 remain pending in the application.

Election/Restrictions

2. Newly submitted claims 20-32 and 34-36 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: above claims raise the new issues: "a circuit for receiving a test vector"; "multiplexer is configured to select between the test vector and the configuration vector"; " a test input for receiving a test vector"; "a second multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan chain elements to select between said first selected vector and a normal operation mode data vector for loading into said scan chain elements"; "means for receiving a test vector"; "means for selecting between the test vector and the configuration vector"; "means for a second multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan chain elements to select between said first selected vector and a normal operation mode data vector for loading into said scan chain elements"; "a method for selecting between a test vector and the configuration vector for loading into the scan chain elements and outputting a first selected vector".

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 20-32 and 34-36 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Amendment

3. The declaration filed on 03/11/2007 under 37 CFR 1.131 has been considered but is ineffective to overcome the Abdollahi's reference.

The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Abdollahi's reference to either a constructive reduction to practice or an actual reduction to practice. The evidence does not include actual pages 24-26 of the mentioned notebook number 1988. Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence must be satisfactorily explained. See 37 CFR 1.131(b), MPEP § 715 .07 and § 2138.06.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-3 and 33 are rejected under 35 U.S.C. 102(a) as being unpatentable by Abdollahi et al. ("Leakage current reduction in sequential circuits by modifying the scan chains", fourth international symposium on 24-28 March 2003").

5. As to claims 1 and 33 Abdollahi discloses:

(1) A circuit, comprising:

circuit elements (pp. 1, 2, 5);

scan chain elements to contain a vector for selective application to said circuit elements (**In the scan-chain design**, the flip-flops are connected in such a way that **they enable two nodes of operation**: **normal node and test mode** – p.2 .. the following steps are used **to apply a test vector**: 1. The circuit is set **into test node by setting *test*=0**. 2, Shift the test vector into flip-flops … 3. The circuit is configured to its **normal node by setting test=1**… - p. 3 … a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1; the **sequential circuit comprises of a combinational circuit and a set of flip-flops** – p.2, Fig.2) (pp. 1, 2, 3);

a vector memory for containing a configuration vector (… **memory** … is used for **storing the MLV/minimum leakage vector** – p. 4) which, when applied to said circuit elements (a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1), configures said circuit elements into **a state** in which a leakage current is reduced (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode** … The **leakage current of a logic gate is a strong function of its input values** … the

input values **affect the number of OFF transistors in NMOS and PMOS** networks of a logic gate. For example, the **minimum leakage current of a two-input NAND gate** corresponds to the case, when **both its inputs are zero**. In this case, **both NMOS transistors** in the MMOS network **are off**, while **both PMOS transistors are on** – p. 2) (pp. 2, 3, 4); and

a multiplexer to select said configuration vector for loading into said scan chain elements (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode. This requires the addition of some multiplexers at the primary inputs of the circuit. The multiplexers are controlled using a sleep signal**. – p. 2 … the scan-based test methodology requires the modification of the circuit and addition of a test mode in which the **flip-flops are configured as one or more scan chains**. … One way to add the new functionality into the flip-flops is through the addition of **a multiplexer with inputs *D* and Ds**, as shown in Fig. 3 … The control input of the multiplexer is controlled by the test signal. This design is referred to as a **multiplexed-input scan** flip-flop – p. 3) (pp. 2-5);

a clock generator to clock said configuration vector into said scan chain elements (A simple way is **to shift in the *MLV***, from a memory (*m+k* bit shift register) into the first *m+k* flip-flops via the *ScanIn* pin by **setting the circuit into the test mode and applying *m+k* clocks**. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After shifting in the MLV, the clock signal can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 – p. 3) (pp. 3-5);

(33) A method for reducing leakage currents in a circuit (a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1), the method comprising:

providing circuit elements (pp. 1, 2, 5);

providing scan chain elements to contain a vector for selective application to said circuit elements (**In the scan-chain design**, the flip-flops are connected in such a way that **they enable two nodes of operation**: **normal node and test mode** – p.2 .. the following steps are used **to apply a test vector**: 1. The circuit is set **into test node by setting *test*=0**. 2, Shift the test vector into flip-flops … 3. The circuit is configured to its **normal node by setting test=1**… - p. 3 … a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1; the **sequential circuit comprises of a combinational circuit and a set of flip-flops** – p.2, Fig.2) (pp. 1, 2, 3);

storing in a vector memory a configuration vector (… **memory** … is used for **storing the MLV/minimum leakage vector** – p. 4) which, when applied to said circuit elements (a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1), configures said circuit elements into **a state** in which a leakage current is reduced (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode** … The **leakage current of a logic gate is a strong function of its input values** … the input values **affect the number of OFF transistors in NMOS and PMOS** networks of a logic gate. For example, the **minimum leakage current of a two-input NAND gate**

corresponds to the case, when **both its inputs are zero**. In this case, **both NMOS transistors** in the MMOS network **are off**, while **both PMOS transistors are on** – p. 2) (pp. 2, 3, 4); and

selecting by a multiplexer to select said configuration vector for loading into said scan chain elements (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode. This requires the addition of some multiplexers at the primary inputs of the circuit. The multiplexers are controlled using a sleep signal**. – p. 2 ... the scan-based test methodology requires the modification of the circuit and addition of a test mode in which the **flip-flops are configured as one or more scan chains**. ... One way to add the new functionality into the flip-flops is through the addition of **a multiplexer with inputs *D* and Ds**, as shown in Fig. 3 ... The control input of the multiplexer is controlled by the test signal. This design is referred to as a **multiplexed-input scan** flip-flop – p. 3) (pp. 2-5);

generating a clocking signal to clock said configuration vector into said scan chain elements (A simple way is **to shift in the *MLV***, from a memory (*m+k* bit shift register) into the first *m+k* flip-flops via the *ScanIn* pin by **setting the circuit into the test mode and applying *m+k* clocks**. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After shifting in the MLV, the clock signal can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 – p. 3) (pp. 3-5);

6. As to claims 2-3 Abdollahi recites:

(2) The circuit of claim 1 further comprising a sleep mode detector (pp. 3-5);

(3) The circuit of claim 2 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements (pp. 3-5).

Remarks

7. The declaration filed on 03/11/2007 under 37 CFR 1.131 has been considered but is ineffective to overcome the Abdollahi's reference.

Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

JACK CHIANG
SUPERVISORY PATENT EXAMINER